

IN THE CLAIMS:

Please amend the claims as follows:

1. (Original) A method of generating a logic design for use in designing an integrated circuit (IC), comprising:

embedding a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design;

wherein the two-dimensional schematic representation includes a set of Register Transfer Diagrams (RTD).

2. (Original) The method of claim 1, further comprising generating the combinatorial one-dimensional logic block.

3. (Original) The method of claim 2, further comprising importing the combinatorial one-dimensional logic block.

4. (Original) The method of claim 3, further comprising following a set of design capture rules.

5. (Original) The method of claim 4, further comprising notifying a designer when capturing data violates the set of design capture rules.

6. (Original) The method of claim 1, further comprising using a set of abstractions.

7. (Original) The method of claim 1, further comprising generating C++ from the unified database.

8. (Currently Amended) The method of claim 7, further comprising generating Verilog from the unified database.

9. (Cancelled)

10. (Original) The method of claim 1, further comprising generating synthesizable Verilog from the unified database.

11. (Original) An article comprising a machine-readable medium which stores executable instructions to generate a logic design for use in designing an integrated circuit (IC), the instructions causing a machine to:

embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design;

wherein the two-dimensional schematic representation includes a set of Register Transfer Diagrams (RTD).

12. (Original) The article of claim 11, further comprising instructions to generate the combinatorial one-dimensional logic block.

13. (Original) The article of claim 12, further comprising instructions to follow a set of design capture rules.

14. (Original) The article of claim 13, further comprising instructions to import the combinatorial one-dimensional logic block.

15. (Original) The article of claim 14, further comprising instructions to notify a designer when capturing data violates the set of design capture rules.

16. (Original) The article of claim 11, further comprising to use a set of abstractions.

17. (Original) The article of claim 11, further comprising instructions to generate C++ from the unified database.

18. (Original) The article of claim 12, further comprising instructions to generate Verilog from the unified database.

19. (Cancelled)

20. (Original) The article of claim 11, further comprising instructions to generate synthesizable Verilog from the unified database.

21. (Original) An apparatus for generating a logic design for use in designing an integrated circuit (IC), comprising:

a memory that stores executable instructions; and

a processor that executes the instructions to:

embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design;

wherein the two-dimensional schematic representation includes a set of Register Transfer Diagrams (RTD).

22. (Original) The apparatus of claim 21, further comprising instructions to generate the combinatorial one-dimensional logic block.

23. (Original) The apparatus of claim 22, further comprising instructions to follow a set of design capture rules.

24. (Original) The apparatus of claim 23, further comprising instructions to import the combinatorial one-dimensional logic block.

25. (Original) The apparatus of claim 24, further comprising instructions to notify a designer when capturing data violates the set of design capture rules.

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Page : 6 of 7

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26. (Original) The apparatus of claim 21, further comprising instructions to use a set of abstractions.

27. (Original) The apparatus of claim 21, further comprising instructions to generate C++ from the unified database.

28. (Currently Amended) The apparatus of claim 27, further comprising instructions to generate Verilog from the unified database.

29. (Cancelled)

30. (Original) The apparatus of claim 29, further comprising instructions to generate synthesizable Verilog from the unified database.
